

Appl. No. 10/783,596  
Amdt Dated Oct. 27, 2005  
Reply to Office Action of July 27, 2005

**Amendments to the Drawings**

The attached sheet of drawing includes changes to FIG 2.

In FIG. 2, parameters --D-- & --H-- have been added.

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### **REMARKS**

Applicant appreciates the Examiner's indication of allowability of claims 14, 18 and 19.

#### **Claim Rejections under 35 U.S.C. 112**

In paragraph [0002], "which screws up" has been amended to "the crosstalk screws up." In paragraph [0003], "enormously" has been changed to "greatly," "the other may need" has been changed to "the other way is," "differential pair b" has been changed to "differential pair." In paragraph [0027] & [0028], --apart-- has been inserted after "are far enough."

In claim 15, "the" has been rewritten as "a". Applicant has redefined the relationship of the "trace" and "level" in the claim 15.

Fig. 2 has been amended to add and denote the parameters "D" & "H." So, rejections under 35 U.S.C. 112 should be withdrawn.

#### **Claim Rejections under 35 U.S.C. 102**

Claims 1,4 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Thornton.

Applicant can not agree with Examiner's allegation that the Thornton also discloses these features because Examiner neglects some facts in the Thornton. Firstly, Thornton discloses that the first and second pairs of conductors (110a, 110b; 114a, 114b) are carried in the cable (108), while the present invention disclosed that the differential pairs are arranged in the printed circuit board having a plurality of layers. These features are NOT disclosed in Thornton. Secondly, Thornton discloses that the components A+, A-, of a first balanced mode signal A are respectively applied to a first pair of conductors 110a, 110b creating a virtual ground plane 112, and the components B+, B-, of a second balanced mode signal B are respectively applied to a second pair of conductors 114a, 114b, and create a virtual ground plane 116. In fact, the conductors 110a, 110b are in the same ground plane 112, and conductors 114a, 114b are in the same ground plane 116.

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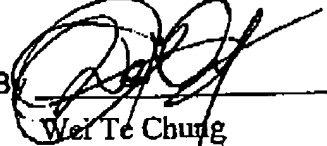
Though the first & fourth conductors (110a, 114b) are disposed in the same level, they are not at the same layer as the present invention. The second & third conductors (110b, 114a) are disposed in the same level, but they are not at the same layer of the present invention. In the present invention, the first signal trace and the second signal trace are disposed in different layers of the PCB. So applicants assert that the structure of the present invention is very different from Thornton.

Applicant has amended claim 1 to include all limitation of claim 4 to overcome rejection by Kazuhiko, therefore, claim 1 should be allowable. Claims 5 should also be allowable since it depends from claim 1 directly.

In view of the foregoing, the subject application as claimed in the pending claims is in a condition for allowance and an action to such effect is earnestly solicited.

Respectfully submitted,

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Appl. No. 10/783,596  
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Appl. No. 10/783,596  
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 Annotated Sheet Showing Changes

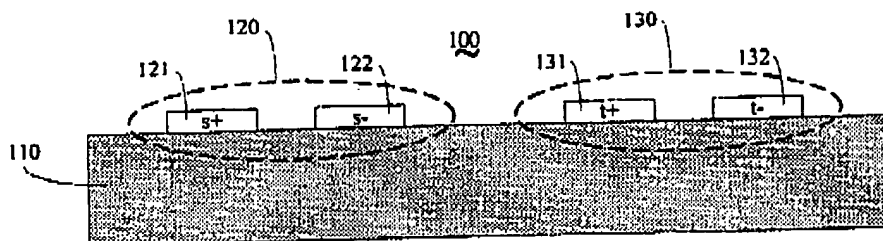


FIGURE 1 (PRIOR ART)

Parameters  $D$  &  $H$  are added.

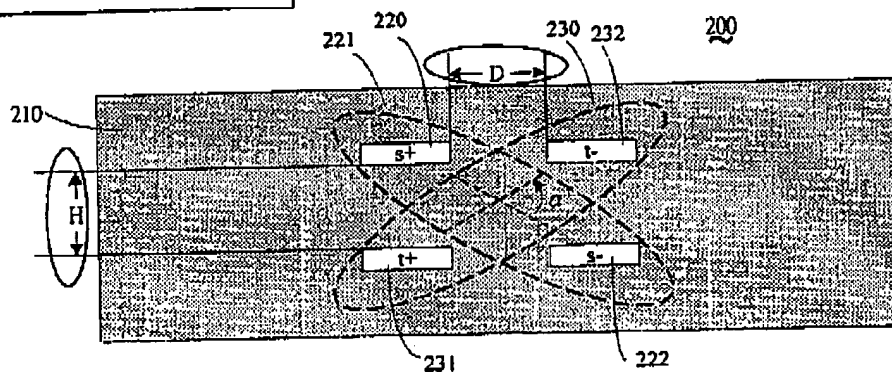


FIGURE 2

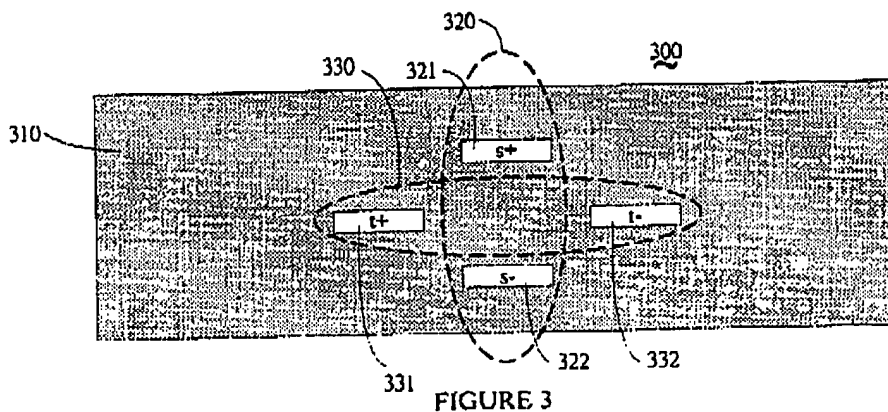


FIGURE 3